

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

- 1 1. (Amended) An input buffer receiver comprising:
  - 2 a buffer input portion for receiving an input signal SIGNAL\_IN, said buffer
  - 3 input portion comprising a bias node;
  - 4 a large capacitor capacitance between a PMOS the bias node and a VSS
  - 5 source lower supply voltage said large capacitor providing a coupling
  - 6 ratio between said large capacitor and a parasitic capacitor coupled
  - 7 between said bias node and a ground reference point approaching a
  - 8 unity value such that a biasing voltage at said biasing node follows
  - 9 said lower supply voltage to minimize effects of a ground noise signal
  - 10 between the lower supply voltage and the ground reference point; and
  - 11 a buffer output portion in communication with the buffer input portion for
  - 12 producing an output signal SIGNAL\_OUT1.
- 1 2. (Amended) The input buffer receiver of claim 1, wherein the buffer input
- 2 portion which receives an the input signal SIGNAL\_IN further comprises:

3 a first transistor of a first conductivity type N11 having a source node to  
4 which a ~~VSS~~ source the lower supply voltage is applied, a gate node to  
5 which a reference voltage ~~VREF~~ is applied, and a drain node at which  
6 the biasing voltage is developed to which a signal VB11 is applied;

7 a second transistor of a second conductivity type P11 having a drain node  
8 which is connected to the drain node of the first transistor ~~N11~~, and a  
9 gate node at which the biasing voltage is developed to which a signal  
10 ~~VB11 is applied~~, and a source node to which an upper supply voltage  
11 source VDD is applied;

12 a third transistor of the second conductivity type P12 having a drain node  
13 which is connected to the drain of a fourth transistor ~~N12~~, a gate node  
14 at which the biasing voltage is developed to which a signal VB11 is  
15 ~~applied~~, and a source node to which ~~an~~ the upper supply voltage  
16 source VDD is applied;

17 a fourth transistor of the first conductivity type N12 having a source node  
18 to which a ~~VSS~~ source lower supply voltage is applied, a gate node to  
19 which an input signal ~~SIGNAL\_IN~~ is applied externally, and a drain  
20 node which is ~~the~~ an input to the buffer output portion.

- 1 3. (Amended) The input buffer receiver of claim 2-4, wherein the first and  
2 fourth transistors, ~~N11 and N12~~, are NMOS transistors, and the second  
3 and third transistors, ~~P11 and P12~~, are PMOS transistors.
- 1 4. (Amended) The input buffer receiver of claim 2-4, wherein the large  
2 capacitor capacitance is connected between the sources of the first and  
3 fourth transistors, ~~N11 and N12~~, of the buffer input portion and the gate of  
4 the second transistor ~~P11~~ of the buffer input portion.
- 1 5. (Amended) The input buffer receiver of claim 2-4, wherein the gate of the  
2 second transistor ~~P11~~ is connected to its drain.
- 1 6. (Amended) The input buffer receiver of claim 2-4, wherein the gate of the  
2 second transistor ~~P11~~ is connected to the drain of the first transistor ~~N11~~.
- 1 7. (Amended) The input buffer receiver of claim 2-4, wherein the gate of the  
2 second transistor ~~P11~~ is connected to the gate of the third transistor ~~P12~~.
- 1 8. (Amended) The input buffer receiver of claim 2-4, wherein the buffer  
2 output portion which produces an output signal SIGNAL\_OUT1 comprises:  
3 a first inverter ~~I11~~ connected to the drain of the third transistor ~~P12~~ and the  
4 drain of the fourth transistor ~~N12~~;

1 9. (Amended) The input buffer receiver of claim 2-4, wherein ~~P12 and N12~~  
2 the third transistor and the fourth transistor activate almost simultaneously  
3 ~~to provide an efficient circuit design technique for filtering~~ minimize the  
4 effects of ground noise on a delay jitter factor of said input buffer.

1 10. (Amended) The input buffer receiver of claim 1, ~~involving a large~~  
2 ~~capacitance coupling ratio, which~~ wherein the large capacitor charge  
3 couples the ~~PMOS~~ bias node of the input buffer receiver to the ~~VSS~~  
4 ~~source~~ lower supply voltage of the input buffer receiver and wherein a  
5 capacitance value of the large capacitor is selected by the formula:-

$$\frac{CHC}{C_p + CHC} \approx 1$$

7 where:

8 CHC is the capacitance value of the large capacitor,

9 and

10 Cp is the capacitance value of the parasitic capacitor.

1 11. (Amended) The input buffer receiver of claim 1, ~~involving a~~ wherein the  
2 capacitance value of the large capacitor relative to said parasitic capacitor

3        ~~capacitance coupling ratio, which~~ results in a quicker response time for the  
4        output signal ~~a SIGNAL\_OUT1.~~

1        12.    (New) An integrated circuit formed on a substrate comprising:

2        an input buffer receiver for receiving an input signal and connected to said  
3        distribution network, said input buffer comprising:

4                    a buffer input portion for receiving the input signal,  
5                    said buffer input portion comprising a bias node;

6                    a large capacitor between the bias node and a lower  
7                    supply voltage, said large capacitor providing a  
8                    coupling ratio between said large capacitor and a  
9                    parasitic capacitor coupled between said bias  
10                   node and a ground reference point approaching a  
11                   unity value such that a biasing voltage at said  
12                   biasing node follows said lower supply voltage to  
13                   minimize effects of a ground noise signal between  
14                   the lower supply voltage and the ground reference  
15                   point ; and

16                   a buffer output portion in communication with the  
17                   buffer input portion for producing an output signal.

- 1    13.    (New) The integrated circuit of claim 12, wherein the buffer input portion of  
2            the input buffer receiver further comprises:
- 3            a first transistor of a first conductivity type having a source node to which  
4            the lower supply voltage is applied, a gate node to which a reference  
5            voltage is applied, and a drain node at which the biasing voltage is  
6            developed ;
- 7            a second transistor of a second conductivity type having a drain node  
8            which is connected to the drain node of the first transistor, and a gate  
9            node at which the biasing voltage is developed, and a source node to  
10           which an upper supply voltage source is applied;
- 11           a third transistor of the second conductivity type having a drain node  
12           which is connected to the drain of a fourth transistor, a gate node at  
13           which the biasing voltage is developed, and a source node to which  
14           the upper supply voltage source is applied;
- 15           a fourth transistor of the first conductivity type having a source node to  
16           which lower supply voltage is applied, a gate node to which an input  
17           signal is applied externally, and a drain node which is an input to the  
18           buffer output portion.

1    14.    (New) The integrated circuit of claim 13, wherein the first and fourth  
2           transistors are NMOS transistors, and the second and third transistors are  
3           PMOS transistors.

1    15.    (New) The integrated circuit of claim 13, wherein the large capacitor is  
2           connected between the sources of the first and fourth transistors of the  
3           buffer input portion and the gate of the second transistor of the buffer input  
4           portion.

1    16.    (New) The integrated circuit of claim 13, wherein the gate of the second  
2           transistor is connected to its drain.

1    17.    (New) The integrated circuit of claim 13, wherein the gate of the second  
2           transistor is connected to the drain of the first transistor.

1    18.    (New) The integrated circuit of claim 13, wherein the gate of the second  
2           transistor is connected to the gate of the third transistor.

1    19.    (New) The integrated circuit of claim 13, wherein the buffer output portion  
2           which produces output signal comprises: a first inverter connected to the  
3           drain of the third transistor and the drain of the fourth transistor;

1 20. (New) The integrated circuit of claim 13, wherein the third transistor and  
2 the fourth transistor activate almost simultaneously to minimize the effects  
3 of ground noise on a delay jitter factor of said input buffer.

1 21. (New) The integrated circuit of claim 12, wherein the large capacitor  
2 charge couples the bias node of the input buffer receiver to the lower  
3 supply voltage of the input buffer receiver and wherein a capacitance  
4 value of the large capacitor is selected by the formula:

5 
$$\frac{CHC}{C_p + CHC} \approx 1$$

6 where:

7 **CHC** is the capacitance value of the large capacitor,  
8 and

9 **C<sub>p</sub>** is the capacitance value of the parasitic capacitor.

1 22. (New) The integrated circuit of claim 12, wherein the capacitance value of  
2 the large capacitor relative to said parasitic capacitor results in a quicker  
3 response time for the output signal.

1 23. (New) A method for minimizing effects of ground noise on an input buffer  
2 receiver comprising the steps of:



3           forming a buffer input portion for receiving an input signal on a substrate;

4           forming a bias node within said buffer input portion;

5           connecting said a lower supply voltage to said buffer input portion;

6           forming a large capacitor between the bias node and the lower supply

7           voltage said large capacitor providing a coupling ratio between said

8           large capacitor and a parasitic capacitor coupled between said bias

9           node and a ground reference point approaching a unity value such that

10          a biasing voltage at said biasing node follows said lower supply voltage

11          to minimize effects of a ground noise signal between the lower supply

12          voltage and the ground reference point; and

13          forming a buffer output portion on said substrate in communication with

14          the buffer input portion for producing an output signal.

1    24.   (New) The method of claim 23, wherein forming the buffer input portion

2           further comprises the steps of:

3           forming a first transistor of a first conductivity type on said substrate;

4           applying the lower supply voltage to a source node of the first transistor;

5           applying a reference voltage to a gate node of the first transistor;

6 connecting a drain node of the first transistor to develop as biasing voltage  
7 at said drain node;

8 forming a second transistor of a second conductivity type on said  
9 substrate;

10 connecting a drain node of the second transistor to the drain node of the  
11 first transistor;

12 connecting a gate node of the second transistor to the drain node of the  
13 first transistor for developing the biasing voltage; and

14 connecting a source node of the second transistor to an upper supply  
15 voltage;

16 forming a third transistor of the second conductivity type on said substrate;

17 connecting a drain node of the third transistor to the drain of a fourth  
18 transistor;

19 connecting a gate node of the third transistor to the drain node of the first  
20 transistor for developing the biasing voltage;

21 connecting a source node of the third transistor to the upper supply  
22 voltage source;

23           forming a fourth transistor of the first conductivity type on said substrate;  
  
24           connecting a source node of the fourth transistor to the lower supply  
25           voltage;  
  
26           connecting a gate node of the fourth transistor to receive an input signal  
27           externally; and  
  
28           connecting a drain node of the fourth transistor to an input to the buffer  
29           output portion.

1    25.   (New) The method of claim 24, wherein the first and fourth transistors are  
2           NMOS transistors, and the second and third transistors are PMOS  
3           transistors.

1    26.   (New) The method of claim 24, wherein forming the large capacitor  
2           comprises the step of:  
  
3           connecting said large capacitor between the sources of the first and fourth  
4           transistors of the buffer input portion and the gate of the second  
5           transistor of the buffer input portion.

1    27.   (New) The method of claim 24, wherein forming the buffer input portion  
2           further comprises the steps of:

3 connecting the gate of the second transistor to its drain.

1 28. (New) The method of claim 24, wherein forming the buffer input portion  
2 further comprises the steps of:

3 connecting the gate of the second transistor to the gate of the third  
4 transistor.

1 29. (New) The method of claim 24, wherein forming the buffer output portion  
2 which produces output signal comprises the step of:

3 forming a first inverter on said substrate; and

4 connecting an input of said first inverter to the drain of the third transistor  
5 and the drain of the fourth transistor;

1 30. (New) The method of claim 24, wherein the third transistor and the fourth  
2 transistor activate almost simultaneously to minimize the effects of ground  
3 noise on a delay jitter factor of said input buffer.

1 31. (New) The method of claim 23, wherein the large capacitor charge  
2 couples the bias node of the input buffer receiver to the lower supply  
3 voltage of the input buffer receiver and wherein a capacitance value of the  
4 large capacitor is selected by the formula:



8 means for forming a large capacitor between the bias node and the lower  
9 supply voltage said large capacitor providing a coupling ratio between  
10 said large capacitor and a parasitic capacitor coupled between said  
11 bias node and a ground reference point approaching a unity value  
12 such that a biasing voltage at said biasing node follows said lower  
13 supply voltage to minimize effects of a ground noise signal between  
14 the lower supply voltage and the ground reference point; and

15 means for forming a buffer output portion on said substrate in  
16 communication with the buffer input portion for producing an output  
17 signal.

1 34. (New) The apparatus of claim 23, wherein forming the buffer input portion  
2 further comprises:

3 means for forming a first transistor of a first conductivity type on said  
4 substrate;

5 means for applying the lower supply voltage to a source node of the first  
6 transistor;

7 means for applying a reference voltage to a gate node of the first  
8 transistor;

9 means for connecting a drain node of the first transistor to develop as  
10 biasing voltage at said drain node;

11 means for forming a second transistor of a second conductivity type on  
12 said substrate;

13 means for connecting a drain node of the second transistor to the drain  
14 node of the first transistor;

15 means for connecting a gate node of the second transistor to the drain  
16 node of the first transistor for developing the biasing voltage; and

17 means for connecting a source node of the second transistor to an upper  
18 supply voltage;

19 means for forming a third transistor of the second conductivity type on said  
20 substrate;

21 means for connecting a drain node of the third transistor to the drain of a  
22 fourth transistor;

23 means for connecting a gate node of the third transistor to the drain node  
24 of the first transistor for developing the biasing voltage;

25 means for connecting a source node of the third transistor to the upper  
26 supply voltage source;

27 means for forming a fourth transistor of the first conductivity type on said  
28 substrate;

29 means for connecting a source node of the fourth transistor to the lower  
30 supply voltage;

31 means for connecting a gate node of the fourth transistor to receive an  
32 input signal externally; and

33 connecting a drain node of the fourth transistor to an input to the buffer  
34 output portion.

1 35. (New) The apparatus of claim 24, wherein the first and fourth transistors  
2 are NMOS transistors, and the second and third transistors are PMOS  
3 transistors.

1 36. (New) The apparatus of claim 24, wherein means for forming the large  
2 capacitor comprises:

3 means for connecting said large capacitor between the sources of the first  
4 and fourth transistors of the buffer input portion and the gate of the  
5 second transistor of the buffer input portion.



1 37. (New) The apparatus of claim 24, wherein means for forming the buffer  
2 input portion further comprises:

3 means for connecting the gate of the second transistor to its drain.

1 38. (New) The apparatus of claim 24, wherein means for forming the buffer  
2 input portion further comprises the steps of:

3 means for connecting the gate of the second transistor to the gate of the  
4 third transistor.

1 39. (New) The apparatus of claim 24, wherein means for forming the buffer  
2 output portion which produces output signal comprises:

3 means for forming a first inverter on said substrate; and

4 means for connecting an input of said first inverter to the drain of the third  
5 transistor and the drain of the fourth transistor;

1 40. (New) The apparatus of claim 24, wherein the third transistor and the  
2 fourth transistor activate almost simultaneously to minimize the effects of  
3 ground noise on a delay jitter factor of said input buffer.

1 41. (New) The apparatus of claim 23, wherein the large capacitor charge  
2 couples the bias node of the input buffer receiver to the lower supply

3 voltage of the input buffer receiver and wherein a capacitance value of the  
4 large capacitor is selected by the formula:

5 
$$\frac{CHC}{C_p + CHC} \approx 1$$

6 where:

7 **CHC** is the capacitance value of the large capacitor  
8 CHC, and

9 **C<sub>p</sub>** is the capacitance value of the parasitic capacitor  
10 C<sub>p</sub>.

1 42. (New) The apparatus of claim 23, wherein the capacitance value of the  
2 large capacitor relative to said parasitic capacitor results in a quicker  
3 response time for the output signal.